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APPLE/FENWICK
SILICON VALLEY CENTER
801 CALIFORNIA STREET
MOUNTAIN VIEW, CA 94041

EXAMINER	
SORRELL, ERON J	

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/667,241
Filing Date: September 18, 2003
Appellant(s): CHRISTIANSEN, KEVIN M.

Brian Brannon (Reg. No. 57,219)
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/26/08 appealing from the Office action mailed 9/18/07.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(**8) Evidence Relied Upon**

5584010	KAWAI et al.	12-1996
5,614,685	MATSUMOTO et al.	03-1997

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawai et al. (U.S. Patent No. 5,584,010 hereinafter “Kawai”) in view of Matsumoto et al. (U.S Patent No. 5,614,685 hereinafter “Matsumoto”).

Referring to apparatus claims 21,26, and 30, and method claim 34, Kawai teaches a memory access controller (see item 103 in figure 6) adapted to be coupled to a computer system memory (see

item 100 in figure 6) and an input/output device (I/O) device (see DSP-2 or DSP-3), comprising:

a register (see item 251 in figure 7) for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a memory (see lines 12-25 of column 9); and

circuitry coupled to the register (see item 260 in figure 7) for receiving the data status signal and for controlling subsequent operation of the memory access controller based on the status signal (see lines 27-51 of column 10).

Kawai fails to teach the data unit is transferred to an external system.

Matsumoto teaches, a system wherein a DSP transfers a data unit to an external system (see lines 60-67 of column 3 and item 12 in figure 1).

All of the claim elements are known in Kawai and Matsumoto. The only difference is the combination of "old elements" into a single device by providing the DSPs taught by Kawai with the data I/O control portion that transfers data from the DSP to an external device taught by Matsumoto by adding the data I/O control portion to the system of Kawai.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to add the

data I/O control portion to the system of Kawai since the data I/O control portion would not affect the operations of the other components of Kawai and the I/O control portion would achieve the predictable results of providing data to an external system for additional processing.

The rejection above is based on the following reasoning: DSP-1 wants to send data to DSP-2 (I/O device), however DSP-2 is busy sending data to the memory, therefore DSP-2 is busy (see figure 10B), once DSP-2 is finished sending data to the external memory, it sends a status signal to the DMA controller of DSP-1 informing DSP-1 that it is now ready to receive data (see lines 15-26 of column 11).

Referring to claims 22 and 27, and method claim 33, Kawai teaches the data status signal indicates the end of a data unit (see lines 31-35 of column 9, note the status is updated to reflect the state of the local bus, if there is a transition from a busy state to a ready state, then there was an end to the previously transferred data unit).

Referring to claims 23 and 28, Kawai teaches the memory controller executes an instruction in response to the data status signal (see lines 11-15 of column 9).

Referring to claims 24 and 29, Kawai teaches the data status signal is used to prompt the memory access controller to request information from the I/O device (see figure 10B, note if the destination, DSP-2 (I/O device) is busy, its continually checked until is becomes ready).

Referring to claim 25, Kawai teaches the data status signal is used to keep the channel process active (see lines 11-15 of column 9, note the channel is kept active with the subsequent data transmission).

Referring to claim 31, Kawai teaches the I/O device generates the status data after a data unit transfer from the computer system memory (see lines 15-26 of column 11). Matsumoto teaches transferring to the system external to the computer system (see lines 60-67 of column 3). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention for the same reasons as mentioned in the rejection of claim 30 above.

Referring to claim 32, Kawai teaches the circuit is capable of using the status data to control any subsequent data unit transfers between the computer system memory (see lines 15-26 of column 11). Matsumoto teaches transferring to the system external to the computer system (see lines 60-67 of column 3). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention for the same reasons as mentioned in the rejection of claim 30 above.

Referring to claim 33, Kawai the memory capable of storing status data is a register (see item 251 in figure 7) and the computer system is a computer (note the computer comprises collectively items 200a-c. the busses and the busses connecting them; this configuration yields, inter alia a system with memory, a data processing unit, a dma controller, an i/o interface, all components of a typical computer).

Referring to claim 36, Kawai teaches determining whether the status data in the status memory indicate completion of the data unit transfer (see figure 10B, note if the destination, DSP-2 (I/O device) is busy, its continually checked until is becomes ready); and transferring another data unit between the memory in

the computer system and the system external to the computer system after determining that the data in the status memory indicate completion of the data transfer (see lines 15-26 of column 11).

(10) Response to Argument

Appellant's argument:

"As the suggested combination of references fails to teach or suggest all of the limitations of the rejection claims, the Examiner's obviousness rejection was improper. Specifically, the suggested combination of Kawai and Matsumoto fails to disclose or suggest "a register that stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," "means for storing a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer system," or "a memory configured to store status data generated by an Input/Output (I/O) device after a data unit transfer between the computer system memory and a system external to the computer system" as variously recited in the independent claims (see page 5 of appellant's brief)."

In support of this argument, the Appellant further argues:

As the Examiner admits...Kawai fails to disclose a register or other storage device which "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," as claimed... Matsumoto does not remedy the deficient disclosure of Kawai. Matsumoto merely discloses a musical tone signal processing device including a central processing unit (CPU), a DSP and a memory (Matsumoto, col. 3, lines 2-10). The DSP includes a data I/O control portion for performing a data input/output control on data transmitted between the DSP and an "external device or system" (Matsumoto, col. 3, lines 60-67). However, Matsumoto only uses the term "external device or system" once in the specification and provides no further description of this term. There is no clarification in Matsumoto of whether the referenced

"external device or system" is external to the system including the DSP or is merely external to the DSP itself. The mere reference in Matsumoto to an "external device or system" without clarification of how the term "external" is used does not disclose "a system external to the computer," as specifically claimed.

Matsumoto does describe an "external data memory," which is separate from the DSP but included in the same system as the DSP (Matsumoto, col. 3, lines 11-22). In view of this disclosure, it appears that Matsumoto uses "external" to describe a device off-chip within the same system as the DSP as opposed to on the same chip as the DSP. There is no disclosure or suggestion that the referenced "external device or system" is different than the "external memory." Further, the "external device or system" is described in conjunction with data communication between the DSP and the data RAM, which, as noted above, is off-chip but not included in a system external to the DSP. As Matsumoto merely discloses different techniques for a DSP to communicate with a memory or other device connected to the DSP via a data bus, nothing in Matsumoto suggests that the use of "external" to describe "device or system" has a different meaning than when used to describe the "data memory." (Matsumoto, FIG. 1; col. 4, lines 1-2). In particular, Matsumoto discloses that the musical tone signal processing device includes an "external data memory, i.e., a data random-access memory (RAM)" which is within the musical tone signal processing device but is external to the DSP. As disclosed in Matsumoto, an "external data memory," depicted by data RAM 14 in Figure 1, communicates with a DSP (Matsumoto, col. 3, lines 11-22). Hence, the use of "external" refers to a memory not on the same chip as the DSP but within the same system as the DSP, processor and memory (Matsumoto, col. 2, lines 2-10). Thus, the "external data memory" disclosed in Matsumoto, like the disclosed processor and memory is only off-chip memory rather than external to the system that includes the DSP. Hence, Matsumoto, like Kawai, merely discloses an off-chip device that is within the same system as the DSP rather than "a system external to the computer," as claimed.

Examiner's Response:

To summarize, the Appellant argues that Matsumoto fails to teach the DSP transmitting data to a system external to the computer,

thus fails to cure the admitted deficiencies of Kawai. The Appellant argues that, considering the entire disclosure of Matsumoto, the RAM (see item 14 in figure 1 of Matsumoto), which is external to the DSP, yet internal to the musical tone generator (the computer) is what is being referred to by "the external device or system" cited by the Examiner as reading on the Appellants "system external to the computer." ***The Examiner disagrees.*** Matsumoto teaches a DSP comprising a data I/O control portion (12) that "performs a data input/output control on data to be transmitted between the DSP and an external device or system." Matsumoto does not specifically define the "external device or system," but that only means that it should be given its plain meaning as would be understood to one of ordinary skill in the art (see MPEP 2111.01). Clearly one of ordinary skill would interpret this to mean a system external to the computer given the disclosure, specifically figure 1, or Matsumoto. One of ordinary skill in the art would not interpret the RAM (item 14 in figure 1) as the external device or system that has data transmitted to it by item 12 of Matsumoto as argued by the Appellant. Matsumoto teaches separate logic for communicating with the RAM (see item 11 and lines 60-61 of column 3), therefore data I/O control portion 12 wouldn't be needed in the system. Given this figure and the related text in

the description, it is reasonable for one of ordinary skill in the art to interpret the "external device or system," taught by Matsumoto to be just that.

The Appellant further argues:

Further, Matsumoto also fails to disclose a register or other storage device which "stores a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer." The data in Matsumoto merely specifies whether to read or write data from memory and does not disclose storing information associated with the completion of a data transfer (Matsumoto, col. 7, lines 56-67). Hence, Matsumoto fails to disclose storing "a data status signal generated by the I/O device after the I/O device transfers a data unit to a system external to the computer," as claimed. In the Final Office Action dated September 18, 2007, the Examiner asserts that "once DSP-2 is finished sending data to the external memory, it sends a status signal to the DMA controller of DSP-1 informing DSP-1 that is it now ready to receive data." See Final Office Action dated September 18, 2007, ¶ 4, page 4. Transferring data between DSP-1 and DSP-2 does not constitute transferring a data unit "to a system external to the computer," as claimed. As disclosed in Kawai, DSP-1 and DSP-2, are both included in the same multi-processor system. See Kawai, FIG. 5, col. 7, lines 1-10. Hence, the status signal cited by the Examiner merely indicates whether different DSPs are transmitting or receiving data. See Kawai, col. 9, lines 12- 25. As Kawai only describes communication between DSPs within a single system, there is no disclosure or suggestion of generating a status signal after transferring data to an external system, as claimed.

Examiner's Response:

The Examiner disagrees. The Appellant is arguing the references individually, at not the combination of references. The Appellant is reminded that one cannot show nonobviousness by

attacking references individually where the rejections are based on combinations of references. *In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., Inc., 800 F.2d 1091, 231 USPQ 375 Fed. Cir. 1986).* The Examiner relies on Kawai to teach the storage device (status register) which stores a data status signal generated by the I/O device after the I/O device transfers a data unit (see rejection of claim 1, supra). Matsumoto is cited to teach a similar device to the cited device of Kawai that teaches sending data units to system external to the computer. The combination of Kawai and Matsumoto allows for a system wherein the storage device stores a data status signal generated by the I/O device after it transfer the data unit (as taught by Kawai) to a system external to the computer (as modified in view of the teachings of Matsumoto).

The Appellant further argues:

Similar to claims 21, 26 and 30, claim 34 recites storing status data after completing a data unit transfer to a system external to the computer system, so the above discussion regarding the deficiencies of Kawai and Matsumoto is hereby incorporated so as to apply to claim 34.

Examiner's Response:

The Appellant has provided no additional arguments with respect to claim 34, therefore the Examiner finds this argument non-persuasive for the same reasons mentioned above.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Eron Sorrell

Examiner 2182

Conferees:

/Manorama Padmanabhan/

QAS, TC2100, WG2180

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182